Hardware/software codesign of a pattern recognition system with on-chip learning

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Abstract - In this paper, we propose a designing method for a hardware implementable pattern recognition system with on-chip learning. The architecture proposed herein takes advantage of distinct modules for controlling the peripherals of the development board and for data processing as forward and backward stages of the propagation and learning phase. The architecture is easily scalable and able to cope with arbitrary network sizes with the same hardware. The entire proposed concept relies on the idea that a FPGAs implementable neural network can be reached only by choosing the predesigned generic blocks and to set the parameters of the network into a pop-up window.

I. Introduction

Signal processing systems for pattern recognition will have to operate in rapidly changing environments. In order to suitably adapt at the varying requirements, control strategies targeted at selecting and tuning the signal processing algorithms need to be developed.

For modeling dynamical systems, as neural networks with on-chip learning, we have designed hardware – software platform powerful and flexible enough to allow ANNs (Artificial Neural Network) of different sizes to be efficiently computed.

We have developed an extendable digital architecture for the implementation of a neural network (NN) with on-chip learning using FPGAs and a design methodology that allows the system designer to concentrate on a high level functional specification.

For this, we have created a new library Simulink block set constituted by Simulink Xilinx blocks, MCode blocks, VHDL blocks and an EDK processor block. With these new blocks, the designer will be able to develop the entire neural network by parameterize the ANN topologies as number of neurons and layers.

The implementation goal is achieved using the Xilinx ISE program in order to generate the VHDL code according to the characteristics of the chosen FPGA device.

II. Pattern Recognition System

The pattern recognition system is made up of neural network processing blocks and an embedded microcontroller block. Both block are hardware implementable and designed in Xilinx System generator respectively in Xilinx Platform Studio. For hardware implementation of the pattern recognition system, the Spartan-3E Starter Board design platform was chosen.

A. Neural network system block

The neural network system designed deals with an extendable digital architecture for the implementation of a multilayer feedforward networks (MLF) using field programmable gate arrays (FPGAs).

The MLP network generally gives quickly results, is efficient with information processing, and learns by presenting examples; but sometimes is difficult to choose the optimal network parameters and training procedures for a given situation. From this reason, the building of a neural network with customizable blocks can give a higher reconfiguration capability and operation of the neural network under real time constraints.

The most difficulty parts in FPGA implementation of the MLP network are the sigmoid function and the calculus algorithm (Delta rule) of the weights.

The parallelism adopted is a node parallelism one and requires managing all the neurons from the same layer in the same time

B. Embedded microcontroller block

In order to control the peripherals of the development board, the MicroBlaze processor was used. The MicroBlaze embedded processor soft core is a reduced instruction set computer (RISC) optimized for implementation in Xilinx Field Programmable Gate Arrays and has been developed to support a high degree of user configurability. This allows tailoring of the processor to meet specific cost/performance requirements. The configuration is done via parameters that typically enable, size, or select certain processor features. In this paper, the used IPs for peripherals are RS-232 port, slide and push-button switches and LCD module.

References

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